Synopsys rolls out DDR Explorer for memory sub-systems

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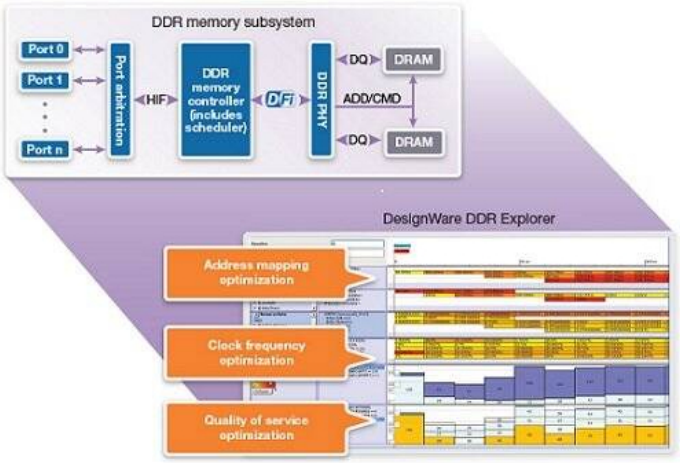
Keywords:DDR Explorer? RTL? DRAM? DesignWare?

Synopsys Inc. unveiled the DesignWare DDR Explorer performance analysis tool, which enables designers to quickly optimise Synopsys' DesignWare Enhanced Universal DDR Memory Controller (uMCTL2) for performance, power and cost.

Using DDR Explorer, designers can analyse their DDR memory sub-system and optimise their architecture to increase efficiency by up to 20 per cent, while achieving 10 times faster turnaround time compared to RTL analysis. With the graphical simulation and analysis provided by DDR Explorer, designers can quickly select the right memory type for the lowest bill of material (BOM) cost and system power. DDR Explorer supports all of the industry standard DRAM interfaces for mobile and enterprise applications, including LPDDR2, LPDDR3, DDR2, DDR3 and DDR4.

DDR Explorer integrates a transaction-level architecture model of the DesignWare DDR Enhanced Universal Memory Controller with a graphical simulation and analysis environment that enables designers to define, run and analyse hundreds of scenarios to identify the best memory controller configuration. RTL-based performance checking, while required for final validation, typically has longer turnaround times and limits the practical number of design explorations during a project to fewer than 25. DDR Explorer enables thorough performance and power sensitivity analysis for over 250 simulations in the same amount of time.



By identifying heavy traffic conditions and bottlenecks, designers can explore the DDR memory controller parameter configurations and register settings to optimise the DDR memory performance. This results in up to 20 per cent greater memory efficiency, lower power consumption and lower memory cost, without sacrificing other memory performance requirements. The optimised configuration from DDR Explorer is used for DDR memory controller RTL IP configuration and performance validation, speeding the implementation and verification of the IP.

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What is RTL?

RTL stands for Register Transfer Level. It is a high-level hardware description language (HDL) used for defining digital circuits. The most popular RTL languages are VHDL and Verilog.

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